CLAIMS

What is claimed as new and desired to be protected by Letters Patent of the United States is:

1. A method for operating a pixel cell of an imager, the method comprising:

accumulating charge at a photoconversion device during an integration period;

storing accumulated charge from said photoconversion device at a charge collection region;

reading out said charge from said charge collection region; and

removing residual charge remaining in said photoconversion device prior to a subsequent integration period.

2. The method of claim 1, wherein said act of removing comprises activating at least one of a reset transistor and a transfer transistor to couple said photoconversion device to a potential prior to said subsequent integration period.

3. The method of claim 2, wherein said reset transistor and said transfer transistor are activated substantially simultaneously.

4. The method of claim 3, wherein said substantially simultaneous activation of said reset transistor and said transfer transistor occurs after said act of reading out said charge.

5. The method of claim 1, wherein said act of transferring comprises transferring charge from said photoconversion device to a floating diffusion region.

6. The method of claim 5, wherein said act of storing charge comprises transferring said charge to said floating diffusion region via said transfer transistor.

7. The method of claim 1, wherein said act of transferring comprises transferring charge from said photoconversion device to a supply voltage Vdd.

8. The method of claim 1, wherein said act of reading out comprises reading out said charge with a transistor.

9. The method of claim 1, wherein the pixel cell is at least one of a five transistor (5T) pixel, a six transistor pixel (6T) or a seven transistor pixel (7T).

10. The method of claim 9, wherein the act of removing comprises activating a transistor electrically connected to said photoconversion device wherein said transistor includes at least one of a global shutter, antiblooming device or high dynamic range transistor (HDR).

11. The method of claim 10, wherein the act of activating said transistor allows residual charge to move from said photoconversion device to a supply voltage (V_{dd}).

12. The method of claim 1, wherein the imager is a CMOS imager.

13. The method of claim 12, wherein the CMOS imager comprises four transistor (4T) pixels.

14. The method of claim 12, wherein the CMOS imager comprises six transistor (6T) pixels.

15. The method of claim 12, wherein the CMOS imager comprises seven transistor (7T) pixels.

16. The method of claim 1, wherein said photoconversion device is a photodiode.

17. The method of claim 1, wherein said photoconversion device is a photogate.

18. The method of claim 1, wherein said photoconversion device is a photoconductor.

19. A method for operating a pixel cell of an imager, the method comprising:

resetting a charge collection region with a reset transistor during a reset period;

accumulating charge at a photoconversion device during an integration period;

storing accumulated charge from said photoconversion device at said charge collection region via a transfer transistor;

reading out said charge from said charge collection region to a sample and hold circuit; and

removing residual charge remaining in said photoconversion device after said charge storage at said charge collection region, wherein said act of removing comprises activating said reset transistor and said transfer transistor prior to a subsequent integration period.

20. The method of claim 19, wherein said act of removing comprises activating said reset transistor and said transfer transistor substantially simultaneously.

21. The method of claim 19, wherein said substantially simultaneous activation of said reset transistor and said transfer transistor occurs after said act of reading out said charge.

22. The method of claim 19, wherein said act of transferring comprises transferring charge from said photoconversion device to a supply voltage Vdd.

23. The method of claim 19, wherein the imager is a CMOS imager.

24. The method of claim 23, wherein the CMOS imager comprises one of a four transistor, five transistor, six transistor or seven transistor pixel architecture.

25. The method of claim 19, wherein said photoconversion device is a photodiode.

26. The method of claim 19, wherein said photoconversion device is a photogate.

27. The method of claim 19, wherein said photoconversion device is a photoconductor.

28. A method for operating a pixel cell of an imager, the method comprising:

resetting a charge collection region with a reset transistor during a reset period;

accumulating charge at a photoconversion device during an integration period;

storing accumulated charge from said photoconversion device at said charge collection region via a transfer transistor;

reading out said charge from said charge collection region to a sample and hold circuit; and

removing residual charge remaining in said photoconversion device after said charge storage at said charge collection region, wherein said act of removing comprises activating a transistor electrically connected to said photoconversion device prior to a subsequent integration period.

29. The method of claim 28, wherein the pixel cell has at least one of a four transistor (4T), five transistor (5T), six transistor (6T) or seven transistor (7T) pixel architecture.

30. The method of claim 28, wherein the act of removing comprises activating said transistor electrically connected to said photoconversion device wherein said transistor includes least one of a global shutter, antiblooming device or high dynamic range transistor (HDR).

31. The method of claim 28, wherein the act of activating said transistor allows residual charge to move from said photoconversion device to a supply voltage (V_{dd}).

32. The method of claim 28, wherein said act of transferring comprises transferring charge from said photoconversion device to a supply voltage Vdd.

33. The method of claim 28, wherein the imager is a CMOS imager.

34. The method of claim 33, wherein the pixel cell is a six transistor (6T) pixel.

35. The method of claim 33, wherein the pixel cell is a seven transistor (7T) pixel.

36. The method of claim 28, wherein said photoconversion device is a photodiode.

37. The method of claim 28, wherein said photoconversion device is a photogate.

38. The method of claim 28, wherein said photoconversion device is a photoconductor.

39. An imaging device, comprising:

a photoconversion device for accumulating charge during an integration period;

a charge collection region coupled to said photoconversion device for storing charge accumulated at said photoconversion device; and

a readout portion coupled to said charge collection region for reading out said charge from said charge collection region, and wherein said imaging device is configured to remove residual charge from said photoconversion device prior to a subsequent integration period.

40. The imaging device of claim 39, further comprising a controller for controlling removal of said residual charge.

41. The imaging device of claim 40, further comprising a reset transistor for resetting said charge collection region to a predetermined state and a transfer transistor for transferring charge from said photoconversion device to said charge collection region, wherein said controller is configured to activate said reset transistor and transfer transistor prior to said subsequent integration period.

42. The imaging device of claim 39, wherein said controller is configured to activate said reset transistor and said transfer transistor substantially simultaneously following said charge readout.

43. The imaging device of claim 39, wherein said imaging device is a CMOS imager.

44. The imaging device of claim 39, wherein said imaging device comprises a four transistor pixel cell.

45. The imaging device of claim 39, wherein said imaging device comprises a five transistor pixel cell.

46. The imaging device of claim 45, further comprising a transistor electrically connected to said photoconversion device.

47. The imaging device of claim 46, wherein said transistor includes at least one of a global shutter, antiblooming device or high dynamic range transistor (HDR).

48. The imaging device of claim 46, wherein said transistor electrically connected to said photoconversion device allows residual charge to move from said photoconversion device to a supply voltage (V_{dd}) when said transistor is activated.

49. The imaging device of claim 39, wherein said charge collection region comprises a floating diffusion region.

50. A processing system comprising:

a processor; and

an imaging device coupled to said processor, said imaging device comprising:

a photoconversion device for accumulating charge during an integration period;

a charge collection region coupled to said photoconversion device for storing charge accumulated at said photoconversion device; and

a readout portion coupled to said charge collection region for reading out said charge from said charge collection region, and wherein said imaging device is configured to remove residual charge from said photoconversion device prior to a subsequent integration period.

51. The system of claim 50, wherein said imaging device further comprises a controller for controlling removal of said residual charge.

52. The system of claim 51, wherein said controller is configured to activate a reset transistor and a transfer transistor prior to said subsequent integration period.

53. The system of claim 52, wherein said controller is configured to activate said reset transistor and said transfer transistor substantially simultaneously following said charge readout.

54. The system of claim 50, wherein said imaging device is a CMOS imager.

55. The system of claim 50, wherein said imaging device comprises a four transistor pixel cell.

56. The system of claim 50, wherein said imaging device comprises a five transistor pixel cell.

57. The system of claim 56, further comprising a transistor electrically connected to said photoconversion device.

58. The system of claim 57, wherein said transistor includes at least one of a global shutter, antiblooming device or high dynamic range transistor (HDR).

59. The system of claim 57, wherein said transistor electrically connected to said photoconversion device allows residual charge to move from said

photoconversion device to a supply voltage (V_{dd}) when said transistor is activated.

60. The system of claim 50, wherein said charge collection region comprises a floating diffusion region.

61. An imager comprising:

an array of pixel sensor cells, said imager being configured to remove residual charge from a respective photoconversion device of each pixel sensor cell included in said imager after a respective signal voltage is readout of each pixel sensor cell and prior to a subsequent integration period for said pixel sensor cell.

62. The imager of claim 61, further comprising a controller for controlling the removal of said residual charge.

63. The imager of claim 62, further comprising a reset transistor and a transfer transistor within each pixel sensor cell and wherein said controller is configured to activate said reset transistor and said transfer transistor substantially simultaneously prior to said subsequent integration period.

64. The imager of claim 62, further comprising a transistor electrically connected to said photoconversion device and wherein said controller is configured to activate said transistor prior to said subsequent integration period.